CLAIMS

What is claimed is:

1. A high speed interconnection link that comprises:

a receiver configured to receive a plurality of channels;

a receiver logic circuit configured to receive signals from each of the plurality of channels and monitor the signals for symbols that are unique to each channel, wherein upon detecting unexpected symbols in the channels, the receiver logic circuit is configured to correct the order of the channels.

2. The link of claim 1, further comprising a transmitter coupled to the plurality of channels and a transmitter logic circuit configured to transmit signals to corresponding channels, wherein the transmitter logic circuit is configured to reorder the correspondence of the signals transmitted to the channels.

3. The link of claim 2, wherein the transmitter logic circuit comprises a bank of multiplexers each configured to transmit a selected one of two input signals to be transmitted through a channel.

4. The link of claim 1, wherein the receiver logic circuit comprises a bank of multiplexers each configured to transmit a selected one of two input signals received from a channel.

5. The link of claim 1, wherein the receiver logic circuit comprises a bank of multiplexers each configured to transmit a selected one of all the signals received in the channels.

6. The link of claim 1, wherein the symbols are insensitive to signal inversion.

7. The link of claim 6, wherein the symbols are 10-bit lane identifiers compatible with an 8B/10B encoding scheme.

8. The link of claim 1, wherein the channel order correction is performed while a first set and a second set of training data are transmitted through the link.

9. The link of claim 8, wherein the training data comprises a binary word sequence that is transmitted across each channel in the link, wherein the first word of the sequence is a comma symbol and the second word of the sequence is the unique channel symbol.

10. A method of correcting the order of data signals received via a plurality of channels, wherein the method comprises:

transmitting symbols across the plurality of channels, wherein the symbols are unique to each channel; and

ordering the channels so that the unique symbols arrive at respective predetermined buffers.

11. The method of claim 10, wherein the plurality of channels are part of a communications link comprising a transmitter port and a receiver port wherein:

the receiver port comprises a lane reorder circuit that is configured to reroute the channel signals if the receiver port detects an unexpected channel symbol in the signals transmitted by the transmitter port; and

a transmit port comprising a lane reorder circuit that is configured to reroute the channel signals if the transmit port does not detect a predetermined response from the receiver port.

12. The method of claim 11, wherein the order of the data signals is corrected during the transmission of a first and a second set of training data, the training data comprising a predetermined sequence of binary words that are transmitted through each channel in the link, wherein at least one of the binary words transmitted through each channel is a unique lane identifier.

13. The method of claim 12 wherein said transmitting includes:

the transmitter port transmitting the first set of training data to the receiver port;

the receiver port transmitting the first set of training data to the transmitter port if the receiver port receives the first set of training data;

the transmitter port transmitting the second set of training data to the receiver port if the transmitter port successfully detects a set of training data from the receiver port; and

the receiver port transmitting the second set of training data to the transmitter port if the receiver port successfully detects a set of training data;

wherein once both ports are transmitting and receiving the second set of training data, correction of the order of data signals in the channels is complete and the link is properly configured to transmit data.

~~14.~~ A computer network that comprises:

a first device having a first adapter;

a second device having a second adapter coupled to the first adapter by a communications link having one or more serial lanes, the second adapter having a multilane transmit path and a multilane receive path, wherein the multilane receive path includes a lane reorder circuit configured to reorder the lanes of the multilane receive path if misordering is detected.

15. The network of claim 14, wherein the multilane receive path further includes:

a plurality of receive buffers coupled via the reorder circuit to the communications link serial lanes; and

a reconstruction circuit configured to retrieve symbols from the plurality of receive buffers to form an output sequence of received symbols, wherein the reconstruction circuit is configured to examine lane identifier symbols in training packets received via the communications link to detect misordering of the lanes.

16. The network of claim 15, wherein when misordering is detected the reorder circuit is configured to adjust the coupling between the serial lanes and the receive buffers to compensate for the misordering.

17. The network of claim 14, wherein the reorder circuit is configured to couple the communication link serial lanes to the lanes of the multilane receive path.

18. The network of claim 14, wherein the first adapter includes a multilane transmit path and a multilane receive path, wherein the multilane receive path includes a lane reorder circuit

configured to reorder the lanes of the multilane receive path if the second adapter is not receiving or is incorrectly receiving signals transmitted from the first adapter to the second adapter.